inputs connected to CK4. The D input of flip-flop 894 is connected to the Q output of flip-flop 888. The D-input of flip-flop 896 is connected to the Q-output of flip-flop 890. The input of inverter 898 is connected to the Q-output of flip-flop 894, and the output of inverter 898 is the SLOW-DOWN2 signal. OR gate 900 provides the SPEED-UP2 signal. One input of OR gate 900 is connected to the Q-output of flip-flop 896, and the other input is connected to the Q-output of flip-flop 892. The SPEED-UP2 and SLOW-DOWN2 signals are connected to the frequency-detector charge pump 824.

In the Abstract:

On page 53, please replace the first paragraph of the Abstract with the following:

A communication system of the present invention utilizes ring detection circuitry on both sides of an isolation barrier. More particularly, the ring detection circuitry may include ring burst circuitry on the phone line side of the isolation barrier and ringer timing circuits on the powered side of the isolation barrier. The digital burst peak signal may be transmitted through the isolation barrier to the ringer timing circuits. By splitting the ring detection circuitry so that the ringer timing circuits are placed on the powered side of the isolation barriers, a significant reduction in the power usage on the phone line side of the barrier related to the ring detection function may occur. The outputs of the ringing timing circuits may be provided to circuits on either side of the isolation barrier. Thus, the ring detection function may be accomplished in a system utilizing an efficient bidirectional capacitive barrier while still minimizing power usage on the line side of the barrier.

Claims 1, 12, 13, 18 and 22 are being amended.

The rewritten clean versions of all the pending claims are provided below. Attached at the end of this paper is an Appendix providing an indication of the changes relative to the prior version of the claims, as now required by Rule 121(c).